Please add the following:

70. (New) An integrated circuit, comprising:

a memory array,

a plurality of sense amplifiers operably connected to the memory array,

an isolation gate operably connected between the memory array and the sense amplifiers, and

a timing circuits operable connected to the isolation gate, comprising:

an input adapted to receive at least one input signal, the at least one input signal including a sense amplifier isolation signal; and

an output connected to an address decoder, wherein the timing circuit activates the address decoder based on the at least one input signal.

71. (New) A timing, integrated circuit, comprising:

an input adapted to receive a row access signal and a sense amplifier isolation signal; and

an output adapted to connect an address decoder, wherein the timing circuit activates the address decoder based on a state of the row access signal and the sense amplifier isolation signal.

72. (New) The timing, integrated circuit according to claim 71, wherein the output presents an activation signal to the address decoder based on the row access signal being low and the sense amplifier isolation signal being low.

73. (New) The timing, integrated circuit according to claim 72, wherein the input includes a NOR gate.

74. (New) The timing, integrated circuit according to claim 72, wherein the input includes an AND gate.

75. (New) An integrated circuit adapted to time activation of a wordline decoder to a sense amplifier isolation signal, comprising:

a first input connected to a sense amplifier isolation signal line;

a second input adapted to receive a memory access control signal;

an output adapted to activate/deactivate a wordline decoder based on the first input and the second input.

76. (New) The integrated circuit of claim 75, wherein the second input receives a row access strobe signal.

77. (New) The integrated circuit of claim 75, wherein the second input receives a low, active signal.

78. (New) The integrated circuit of claim 75, further comprising a logic element that produces an output signal on the output based on the first input and the second input.

79. (New) A timing circuit, comprising:

a delay circuit connected to a sense amplifier isolation signal line;

a first input connected to the delay circuit;

a second input adapted to receive at least one input signal; and

an output based on the first input and the second input and connected to an address decoder, wherein the timing circuit activates the address decoder based on the first input signal and the second input signal.

80. (New) The timing circuit of claim 79, wherein the delay circuit includes a programmable delay.

81. (New) The timing circuit of claim 80, wherein the programmable delay is within a range of programmable delay times.

82. (New) The timing circuit of claim 81, wherein the range of programmable delay times represents the propagation time of a sense amplifier isolation signal on the sense amplifier signal line.

83. (New) The timing circuit of claim 79, wherein the delay circuit is adapted to produce a delay based on a propagation time of an isolation signal.

84. (New) The timing circuit of claim 79, wherein the delay circuit is adapted to produce a delay based on a signal required for accessing a wordline, column or memory location in a memory device.

85. (New) An integrated circuit adapted to time activation of a wordline decoder to a sense amplifier isolation signal, comprising:

a first input adapted to receive a sense amplifier isolation signal;

a second input adapted to receive a memory access control signal;

a timing output adapted to activate/deactivate a wordline decoder based on the first input and the second input.

86. (New) The integrated circuit of claim 85, wherein the first input is active, the second input is inactive and the timing output is inactive.

87. (New) The integrated circuit of claim 86, wherein the first input is active at a high state and the second input is active at a low state.

88. (New) The integrated circuit of claim 85, wherein the timing output produces an active signal with the first input being low and the second input being low.